

WHAT IS CLAIMED:

1. A phase-lock loop comprising:
  - an oscillator having an oscillator signal whose frequency is related to a received error correction signal;
  - a phase-frequency detector receiving and comparing the oscillator signal and a reference signal from the master circuit and generating the error correction signal based on the phase difference of the oscillator signal and the reference signal;
  - a first window circuit which counts the number of comparing cycles of the detector and provides a first window signal for the transmission of the error correction signals from the detector to the oscillator at a frequency of a predetermined number of counted comparing cycles; and
  - a second window circuit which, in response to at least the oscillator signal, narrows the first window signal to limit the duration of the correction signal for irregular reference signals.
2. The phase-lock loop according to Claim 1, wherein the second window circuit is responsive to both the oscillator signal and the reference signal.
3. The phase-lock loop according to Claim 2, wherein the second window circuit includes, for each of the oscillator signal and the reference signal, a delayed path delayed with respect to a generally non-delayed path for the respective signal and a first logic circuit responsive to the delayed and the generally non-delayed signals to produce a second window signal which narrows the first window signal.
4. The phase-lock loop according to Claim 3, wherein the delayed paths provide the delayed oscillator signal and reference signal for comparing.
5. The phase-lock loop according to Claim 3, including a second logic circuit responsive to the first and second window signals to transmit the error correction signals from the detector to the oscillator.
6. The phase-lock loop according to Claim 3, wherein the delayed paths each include an inverter.

7. The phase-lock loop according to Claim 1, wherein the second window circuit includes a delayed path delayed with respect to a generally non-delayed path for the respective signal and a first logic circuit responsive to the delayed and non-delayed signals to produce a second window signal which narrows the first window signal.

8. The phase-lock loop according to Claim 7, including a second logic circuit responsive to the first and second window signals to transmit the error correction signals from the detector to the oscillator.

9. The phase-lock loop according to Claim 7, wherein the delayed path includes an inverter.

10. The phase-lock loop according to Claim 1, including a charge pump between the detector and the oscillator; the detector provides the error correction signals as up and down signals on separate paths; and the first and second window circuits control the transmission of the up and down signals to the charge pump.

11. The phase-lock loop according to Claim 1, including a rate selector circuit which monitors and adjusts the predetermined number of counts as a function of the error correction signal.

12. A pulse width modulated system having a master and a slave controller, the slave controller having a phase-lock loop which comprises:

an oscillator having a PWM signal whose frequency is related to a received error correction signal;

a phase-frequency detector receiving and comparing the PWM signal and a reference signal from the master circuit and generating the error correction signal based on the phase difference of the oscillator signal and the reference signal;

a first window circuit which counts the number of comparing cycles of the detector and provides a first window signal for the transmission of the error correction signals from the detector to the oscillator; and

a second window circuit which, in response to at least the PWM signal, narrows the first window signal to limit the duration of the correction signal for irregular reference signals from the master controller.

13. The system according to Claim 12, wherein the second window circuit is responsive to both the PWM signal and the reference signal.

14. The system according to Claim 13, wherein the second window circuit includes, for each of the PWM signal and the reference signal, a delayed path delayed with respect to a generally non-delayed path for the respective signal and a first logic circuit responsive to the delayed and non-delayed signals to produce a second window signal which narrows the first window signal.

15. The system according to Claim 14, wherein the delayed paths provide the delayed PWM signal and reference signal for comparing.

16. The system according to Claim 14, including a second logic circuit responsive to the first and second window signals to transmit the error correction signals from the detector to the oscillator.

17. The system according to Claim 14, wherein the delayed paths each include an inverter.

18. The system according to Claim 12, wherein the second window circuit includes a delayed path delayed with respect to a generally non-delayed path for the respective signal and a first logic circuit responsive to the delayed and non-delayed signals to produce a second window signal which narrows the first window signal.

19. The system according to Claim 18, including a second logic circuit responsive to the first and second window signals to transmit the error correction signals from the detector to the oscillator.

20. The system according to Claim 18, wherein the delayed path includes an inverter.

21. The system according to Claim 12, including a charge pump between the detector and the oscillator; the detector provides the error correction signals as up and down signals on separate paths; and the first and second window circuits control the transmission of the up and down signals to the charge pump.

22. The system according to Claim 12, including a rate selector circuit which monitors and adjusts the predetermined number of counts as a function of the error correction signal.

23. A pulse width modulation controller including a phase-lock loop according to Claim 1; and wherein the reference signal is a master PWM signal, and the oscillator signal is a slave PWM signal of the controller.

24. A power supply circuit comprising:  
a main power supply;  
a master PWM power supply that generates a first regulated supply voltage and a master PWM signal; and  
a slave PWM power supply that receives the master PWM signal and generates a second regulated supply voltage and includes a phase-lock loop; and  
wherein the phase-lock loop is according to Claim 1 and wherein the reference signal is the master PWM signal and the oscillator signal is a slave PWM signal used to regulate the second regulated supply voltage.

25. A transmitter/receiver comprising:  
a receiver circuit which generates a received base-band data signal from a modulated received signal and a local oscillator signal;  
a transmitter circuit which generates a modulated transmission signal from a transmission base-band data signal and a local oscillator signal; and  
a phase-lock loop coupled to the receiver and transmitter circuits; and  
wherein the phase-lock loop is according to Claim 1.

26. A computer system comprising:  
a central processing unit connected to a bus system;  
a video processor connected to the bus system, controlled by the central  
processing unit and including a power supply circuit;  
a display device connected to the video processor; and  
wherein the power supply circuit is according to Claim 24.